REMARKS:

Claims 1-12 were pending in the application. By this amendment, claims 1 and 2 are being cancelled, without prejudice, and claim 3 is being rewritten in independent form. No new matter is involved. Reconsideration and allowance in view of this amendment and the following remarks are respectfully requested.

In previously rejecting claim 3 on the basis of Shinada, the Examiner states on page 4 of the final Office Action of March 1, 2002 that Shinada discloses that "the system control circuit synchronizes the recording data to be newly recorded onto the disk" and the "data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk". However, in Shinada, a disk is reproduced in order to obtain data to be recorded onto the disk. Reproduction and recording are alternatively performed in Shinada for this purpose, and Shinada fails to disclose or suggest the idea of reproducing the disk for the purpose of setting the timing for additional recording onto the disk so that the additional recording follows the data recorded immediately before the suspension of recording.

On the other hand, in the case of the present invention, the data to be recorded, which is output from an encoder, is synchronized to data already recorded onto the disk in order to allow additional recording continuously from a position so that there is no gap from the data recorded immediately before suspension of recording. In this connection, see line 23 of page 11 through line 5 of page 12 of the specification.

Therefore, claim 3 is submitted to clearly distinguish patentably over the prior art. Claims 4, 5 and 6 depend from and contain all of the limitations of claim 3, so as to also distinguish patentably over the art.

For the reasons previously pointed out, independent claim 7 is submitted to clearly distinguish patentably over the art. Claims 8-12 depend, directly or indirectly, from claim 7 and contain all of the limitations thereof, so that such claims are also submitted to distinguish patentably over the art.

Therefore, reconsideration and allowance are respectfully requested.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: June 27, 2002

By: _____
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

Version with markings to show changes made:

3. (Twice Amended) [A recording data processing device according to claim 2, wherein]A recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a disk, comprising:

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory;

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit, and

a writing circuit for writing the recorded data supplied from the data processing circuit, onto the disk,

wherein

the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock,

wherein

the system control circuit stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address,

and wherein

the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being

operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.